

ASSIGNMENT # 6

CHAPTER 7

7.14 Consider a mem hierarchy using one of the 3 organizations for main memory in Figure 7.11 on page 489. Assume the following:

Cache block size is 16 words,

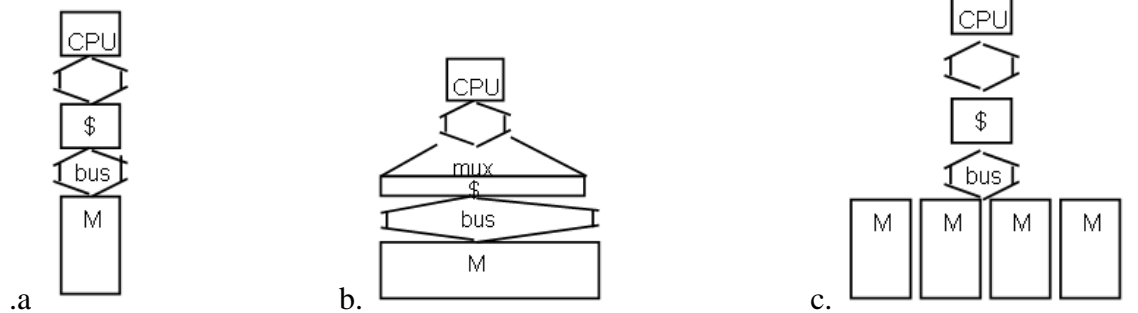
Width of organization (b) of the figure is 4 words

Number of banks in organization (c) is 4

Main memory latency for new access is 10 memory bus clock cycles

Transfer time is 1 memory bus clock cycle

What are the miss penalties for each of these organizations?



7.46 The following C program could be used to help construct a cache simulator. Many of the data types have not been defined, but the code accurately describes the actions that take place during a read access to a direct-mapped cache.

```
word ReadDirectMappedCache(address a)
    static Entry cache[CACHE_SIZE_IN_WORDS];
    Entry e = cache[a.index]
    if (e.valid == FALSE || e.tag != a.tag)
    {
        e.valid = true;
        e.tag = a.tag;
        e.data = load_from_memory(a);
    }
    return e.data;
```

Your task is to modify this code to produce an accurate description of the actions that take place during a read access to a direct-mapped cache with multiple-word blocks.

7.52 Why might a compiler perform the following optimization?

```
/* Before */  
for (j=0; j<20; j++)  
    for(i=0; i<200; i++)  
        x[i][j] = x[i][j]+1;
```

```
/* After */  
for (i=0; i<200; i++)  
    for(j=0; j<20; j++)  
        x[i][j] = x[i][j] +1;
```