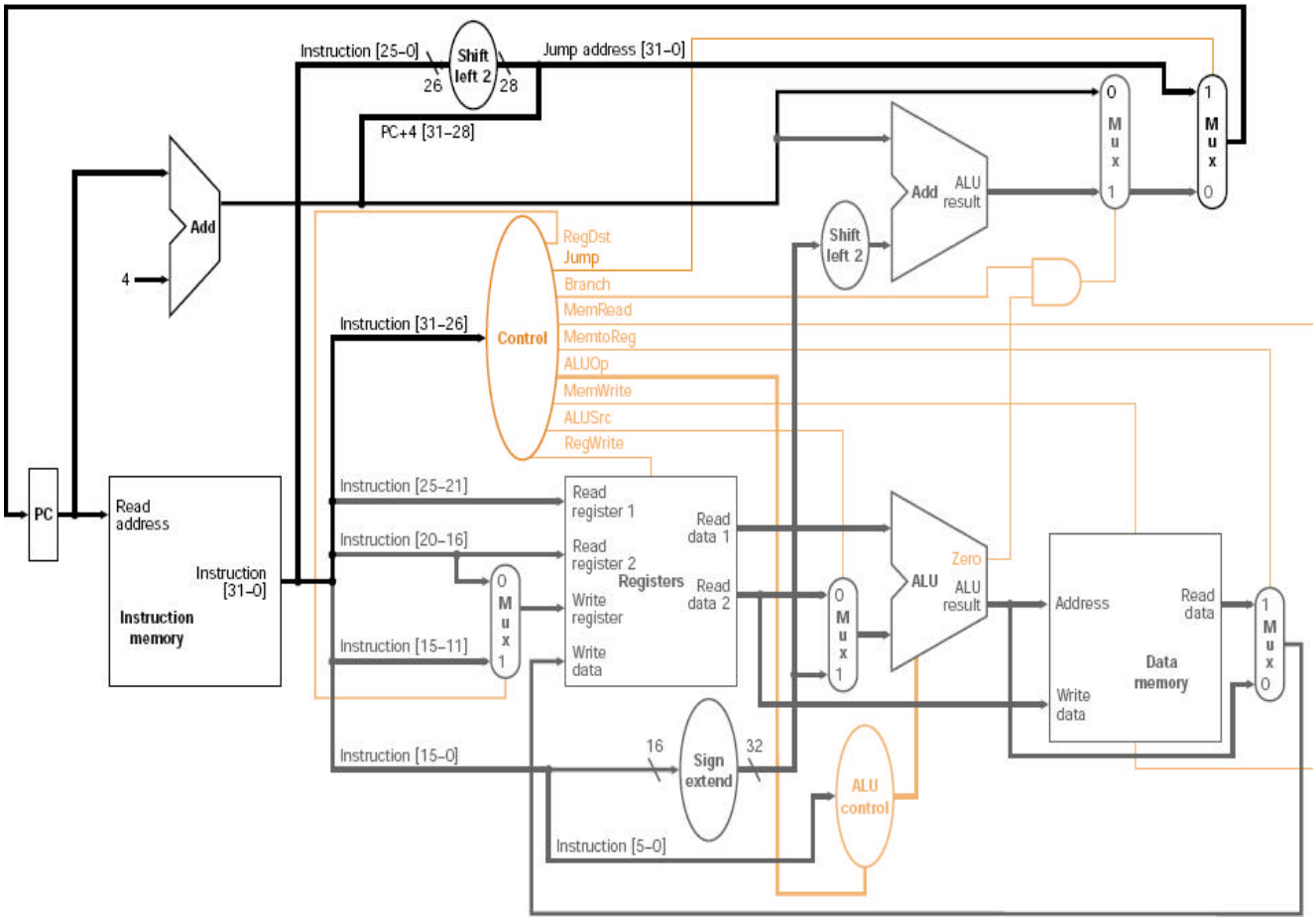
CPE 442
HW#3

5.8 Show the needed changes to the single cycle processor design of MIPS shown below to support the jump register instruction Jr of the MIPS instruction set architecture.



5.10 Show the needed changes to the above single cycle processor design of MIPS shown below to support the load upper immediate LUI instruction of the MIPS instruction set architecture.

5.13 Consider the above cycle processor design of MIPS, a friend is proposing to modify it by eliminating the control signal MemroReg. The multiplexer that has the MemtoReg as an input will instead use either the ALUSrc or the MemRead control signal. Will your friend's modification work? Can one of these two signals (MemRead and ALUSrc) substitute for each other? Explain.

5.28 The concept of the "critical path" , the longest possible path in the machine, was introduced in 5.4 on page 315. Based on your understanding of the single-cycle implementation, show which units can tolerate more delays (i.e. are not on the critical path), and which units can benefit from hardware optimization. Quantify your answers taking the same numbers presented on page 315